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EXAMINER

DANG, KHANH

| ART UNIT | PAPER NUMBER |
|----------|--------------|
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2111

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

87

Office Action Summary

Application No.

10/032,248

Applicant(s)

LI, GABRIEL

Examiner

Khanh Dang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, '1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 6-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 21 and 22 is/are allowed.
- 6) ☒ Claim(s) 1-3 and 6-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 7, 9, 11-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Dodd et al. (6,530,006).

At the outset, it is noted that similar claims will be grouped together to avoid repetition.

As broadly drafted, these claims do not define any structure that differs from Dodd et al. (Dodd).

With regard to claim 1, Dodd discloses a high speed serial memory interface system comprising: an information configuration core (120) for coordinating proper alignment of information communication signals; a system interface (memory controller 110/120 interface) for communicating with a system controller (110), said system interface coupled to said information configuration core (120); and a memory array interface (120/memory array interface) for communicating with a memory array (130/135 or 1-8), said memory array interface coupled to said information core (120). Previously added limitations to the claims are addressed below, under "Response to Arguments."

With regard to claim 2, the system interface of Dodd comprises: a serial read data port (it is clear that the data buffers 123/124 must include read data port for communication with the read information from controller 110) for communicating serial read information from said system controller, said serial read data port communicates said serial read information in accordance with a first synchronized clock signal (the clock for controller 110); a serial write data port (it is clear that the data buffers 123/124 must include write data port for communication with the write information from controller 110) for communicating serial write information from said system controller (110), said serial write data port communicates said serial write information in accordance with said first synchronized clock signal (clock for controller 110); and a serial address data port (it is clear that the data buffers 123/124 must include write data port for communication with the address information from controller 110) for communicating serial address information from said system controller (110), said serial address data port communicates said serial address information in accordance with said first synchronized clock signal (clock for controller 110).

With regard to claim 3, the memory array interface of Dodd comprises: a parallel transmit port (it is clear that the buffers 123/124 must include a parallel transmit port, see additionally Fig. 5, see also col. 2, lines 54-63) for transmitting information to said memory array (1-8, for example), said parallel transmit port transmits said information in accordance with a second synchronized clock signal (clock for memory devices 130/135 or 1-8); a parallel receive port for receiving information from said memory array (it is clear that the buffers 123/124 must include a parallel receive port, see additionally Fig.

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5, see also col. 2, lines 54-63), said parallel receive port receives said information in accordance with a second synchronized clock signal (clock for memory devices 130/135 or 1-8); a parallel address port (it is clear that the buffers 123/124 must include a parallel address port, see additionally Fig. 5, see also col. 2, lines 54-63) for communicating address information to an address array, said parallel address port communicates said address information in accordance with a second synchronized clock signal (clock for memory devices 130/135 or 1-8); and a control port (for communicating control information to said memory array, said control port (it is clear that the buffers 123/124 must include a control port, see additionally Fig. 5, see also col. 2, lines 54-63) communicates said control information in accordance with a second synchronized clock signal (clock for memory devices 130/135 or 1-8).

With regard to claims 6 and 9, it is clear that the memory clock is slower than the controller clock.

With regard to claim 7, note address and control/command buses and data buses to and from memory devices (130/135 or 1-8).

With regard to claims 11, 12, and 16, see discussion above. Note also that Dodd additionally disclose a "single chip memory module integrated high speed interface system." See at least Fig. 5 and description thereof. Newly added limitations to the claims will be addressed below, under "Response to Arguments."

With regard to claims 13 and 14, the alleged advantages are irrelevant and do not define any step/structure that differs from Dodd.

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With regard to claim 15, as in any memory system, in Dodd, the data and address bits are provided synchronously upon a clock signal edge.

With regard to claims 17-20, it is clear that one using the system of Dodd would have performed the same steps set forth in claims 17-20. Newly added limitations to the claims will be addressed below, under "Response to Arguments."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dodd.

Dodd, as discussed above, discloses the claimed invention except for the use of DDR (double data rate) or "double data rated clocking." However, DDR clocking is old and well-known for its use to send data synchronously with the clock pulse signal using the double-data-rate method (DDR); wherein data transfer occurs during both the rising and the falling edges of the clock pulse. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use DDR clocking, since the Examiner takes Official Notice that the use of DDR method is old and well-known and providing DDR clocking to Dodd only involves ordinary skill in the art. If Applicant chooses to properly challenge the Official Notice, supportive document(s) will be provided upon request.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dodd.

Dodd, as discussed above, discloses the claimed invention except for the use of 8B/10B encoder. However, 8B/10B encoder is old and well-known for its use in serial data transmission standards to make sure there are enough transitions in the serial data stream so the clock can be recovered easily. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use 8b/10b encoder, since the Examiner takes Official Notice that the use 8B/10B encoder is old and well-known and providing 8B/10B encoder to Dodd only involves ordinary skill in the art. If Applicant chooses to properly challenge the Official Notice, supportive document(s) will be provided upon request.

Response to Arguments

Applicants' arguments filed 8/24/2004 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris*, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997). In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read

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into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 102 Rejection:

With regard to claims 1, 11, and 17, Applicants argue that “Dodd et al. reference does not teach communication at a first communication rate and a second communication rate. Furthermore, Applicant again respectfully reasserts the Dodd et al. reference teaches away by indicating the frequency and phase of the input and output signal are the same (Col. 5, lines 27 – 30). The present Office Action indicates the ‘Examiner disagrees’. Applicant respectfully asserts the Dodd et al. reference indicates ‘When the PLL is “locked” the frequency and phase of the output signal are the same as those of the input signal’.” Contrary to Applicants’ argument, Dodd et al. never teaches that the operating frequency of the system interface at one side of the information configuration core 120 is always the same as the operating frequency of the memory interface at the other side of information configuration core 120 communicating with the memory array. Column 5, lines 27-32 clearly states that “[w]hen the PLL is ‘locked,’ the frequency and phase of the output signal are the same as those of the input signal. If the phase of the input signal varies, the phase of the output signal follows” (emphasis

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added). It is clear that if the input and output are operated at the same frequency or, in other words, there is no variation in frequency and phase between the input and output, then there is absolutely no need to use a PLL to compensate/control the difference in "rate" by phase alignment in order to prevent clock skew.

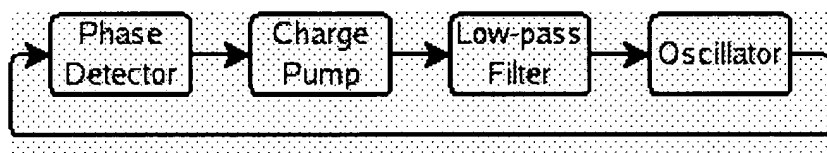
Applicants also state that "[t]he present Office Action also indicates '... Dodd clearly states that 'there is a need for a system and method to provide a memory system that would not only provide reliable transmission and reduce clock insertion and propagation delay, but also would not require each component to operate with the same interface voltage and frequency'" and further state that "the acknowledgement in the present Office Action that a there is a need for a system that would not require each component to operate with the same interface voltage and frequency seems to teach away from conventional systems always inherently have different frequencies because if the conventional systems always have different frequencies there would not be a need for them to require each component to operate at the same frequency if the conventional systems already operated at different frequencies." In response to Applicants' argument, it is acknowledged that Applicants concede that Dodd et al. discloses "there is a need for a system and method to provide a memory system that would not only provide reliable transmission and reduce clock insertion and propagation delay, but also would not require each component to operate with the same interface voltage and frequency." It is also noted that Applicants' argument is irrelevant and/or does not relate to any specific claim language.

Applicants argue that “[e]ven if the Dodd et al. reference mention of different frequencies can be interpreted in another manner, Applicant respectfully asserts that the Dodd et al. reference still teaches away from the present invention anyway by indicating that external (discrete) buffers (Co1. 3, lines 40 – 45) are utilized to allow different frequencies rather than buffers on a single substrate. Contrary to Applicants’ argument, Dodd et al., column 3, lines 40-45, clearly states that the buffers can be placed on a motherboard or on external (discrete buffers).” It is clear from at least Fig. 5 of Dodd et al. that the memory array (1-8) is included on a same substrate as the high speed serial memory interface system (included in memory module 150). See also Dodd, column 3, lines 18-31.

As already discussed in the previous Office Action, it is clear that the system interface at one side of the information configuration core 120 communicates with system input clock 10 of the memory controller at one rate; and the memory interface at the other side of information configuration core 120 communicates with the memory array at another rate; and the Delay Locked Loop (see column 4, line 42 to column 5, line 5), Phase Locked Loop (see column 5, lines 6-32), or Delay Chain (column 5, lines 45-56) to compensate/control the difference in “rate” by phase alignment in order to prevent clock skew. Still further, Dodd et al. discloses that the memory controller (communicating with the system interface at one side of the information configuration core 120 and the memory array 130-145, 170-185 (communicating with the memory interface at the other side of the information configuration core 120) are operated at different voltages and frequencies (see column 3, lines 42-45). Applicants further argue

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that in Dodd, the Delay Locked Loop, Phase Locked Loop, or Delay Chain are used to adjust or correct phase shifts and/or clock skew due to a propagation delay and not a rate or frequency difference. Contrary to Applicants' argument, the following is a basic Phase Locked Loop:



Many systems use internal clocks which are required to be phase-aligned to and/or frequency multiples of some external reference clock. For example, a typical PC controller might have an internal 2.4 GHz core clock which is phase aligned to a bus clock running at 100 MHz. The frequency multiplication is important because multiplying frequencies on chip is much easier than transmitting high frequency clocks on a motherboard. The phase alignment is important so that data can be exchanged reliably between circuits in the high frequency core domain and circuits in the lower frequency bus clock domain. The circuit which synthesizes the high frequency core clock from and phase aligned to the bus clock is called a Phase-Locked Loop. See a detailed definition of Phase Locked Loop by Wikipedia, provided below. The examiner also maintains the position that in a typical computer system, the system clock is higher than the memory clock and lower than the CPU clock. As a matter of fact, Dodd clearly states that "there is a need for a system and method to provide a memory system that would not only

provide reliable transmission and reduce clock-insertion and propagation delay, but also would not require each component to operate with the same interface voltage and frequency" (emphasis added). In response to Applicants' argument regarding the use of buffers in Dodd, it is clear from Dodd that buffers with embedded clock circuit is employed because of the difference in speed/rate/frequency between different components.

With regard to claims 2 and 3, in response to Applicants' argument, it is clear from at least Figs. 1, 2, and 5 of Dodd et al. that the system interface at one side of the information configuration core 120 communicates with the memory controller 110 in series whereas the memory interface at the other side of the information configuration core 120 communicates with the memory array in parallel. Further, it is clearly inherent that ports must be provided for the series or parallel connections. Further, it is clear that the system interface at one side of the information configuration core 120 communicates with system input clock 10 of the memory controller at one rate; and the memory interface at the other side of information configuration core 120 communicates with the memory array at another rate; and the Delay Locked Loop (see column 4, line 42 to column 5, line 5), Phase Locked Loop (see column 5, lines 6-32), or Delay Chain (column 5, lines 45-56) to compensate/control the difference in "rate" by phase alignment in order to prevent clock skew.

With regard to claim 6, Applicants argue that "Dodd et al. reference does not teach the memory array interface operates at a second clock speed that is slower than a first clock speed of operations at the system interface. In addition, Applicant

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respectfully asserts the Dodd et al. reference emphasis teaches away from the present invention by indicating the input clock to the memory array is the same as the controller clock (Co1. 3 lines 67 - Col. 4 line 51) and when the PLL is locked the frequency and phase of the output signal are the same as those of the input signal (Co1. 5, lines 28 – 30).” The Examiner disagrees. It is inherent that in a conventional system, the system clock is always higher than the memory clock. In particular, the memory clock is clearly lower than the system clock as disclosed by Dodd et al. Further, and the memory interface at the other side of information configuration core 120 communicates with the memory array at another rate; and the Delay Lock Loop (see column 4, line 42 to column 5, line 5), Phase Lock Loop (see column 5, lines 6-32), or Delay Chain (column 5, lines 45-56) to compensate/control the difference in “rate” by phase alignment in order to prevent clock skew. Many systems use internal clocks which are required to be phase-aligned to and/or frequency multiples of some external reference clock. For example, a typical PC controller might have an internal 2.4 GHz core clock which is phase aligned to a bus clock running at 100 MHz. The frequency multiplication is important because multiplying frequencies on chip is much easier than transmitting high frequency clocks on a motherboard. The phase alignment is important so that data can be exchanged reliably between circuits in the high frequency core domain and circuits in the lower frequency bus clock domain. The circuit which synthesizes the high frequency core clock from and phase aligned to the bus clock is called a Phase-Locked Loop. The examiner also maintains the position that in a typical computer system, the system clock is higher than the memory clock and lower than the CPU clock. As a matter of fact,

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Dodd clearly states that “there is a need for a system and method to provide a memory system that would not only provide reliable transmission and reduce clock-insertion and propagation delay, but also would not require each component to operate with the same interface voltage and frequency” (emphasis added). In response to Applicants’ argument regarding the use of buffers in Dodd, it is clear from Dodd that buffers with embedded clock circuit is employed because of the difference in speed/rate/frequency between different components.

With regard to claim 7, see address and control/command buses and data buses to and from memory devices (130/135 or 1-8). As a matter of fact, for a memory array to work, reading and writing of data from a memory must be performed using address and control buses.

With regard to claims 13 and 14, it is still the Examiner’s position that the alleged advantages are irrelevant and do not define any step/structure that differs from Dodd.

With respect to claims 11, 12, and 16, Applicants argue that “the Dodd et al. reference does not teach a single chip memory module.” Contrary to Applicants’ argument, it is clear from at least Fig. 5 and column 3, lines 18-31 of Dodd et al. the memory module 150 is a “single chip.” And just like the “single chip” claimed in claim 11, the module 150 also comprises a memory module array (1-8), and information configuration core 120. In response to Applicants’ argument with respect to Claims 13 and 14, the Examiner maintains his position that the alleged advantages are irrelevant and do not define any step/structure that differs from Dodd et al. Since Dodd et al.

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meets all claimed structural limitations, the alleged advantages such as manageable capacitive flux or noise reduction are readily realized.

With regard to claim 15, the Examiner maintains his position that as in any memory system, in Dodd, the data and address bits are provided synchronously upon a clock signal edge.

With regard to claims 17-20, it is still the Examiner's position that it is clear that one using the system of Dodd would have performed the same steps set forth in claims 17-20.

The 103 Rejection:

With regard to claims 8 and 10, Applicants appear to argue that even if the DDR and 8B/10B encoder is old and well-known, the combination as claimed is not obvious or there's no motivation to combine or modify. In response, it is clear that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In the instant case, the DDR clocking is old and well-known in the art for its use to send data synchronously with the clock pulse signal using the double-data-rate method (DDR); wherein data transfer occurs during both the rising and the falling edges of the clock pulse. The 8B/10B encoder is old and well-known in the art for its

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use in serial data transmission standards to make sure there are enough transitions in the serial data stream so the clock can be recovered easily. As stated in the Wikipedia's definition of Phase Locked Loop, it is very common to use 8B/10B encoder with Phase Locked Loop.

Allowable Subject Matter

Claims 21 and 22 are allowed.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang

Khanh Dang
Primary Examiner